9328

MSI DUAL 8-BIT SHIFT REGISTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9328 is a high speed serial storage element providing sixteen bits of storage in the form of two eight bit registers that will shift at greater than 20 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each eight bit register, and both registers may be master cleared from a common input.

FEATURES:

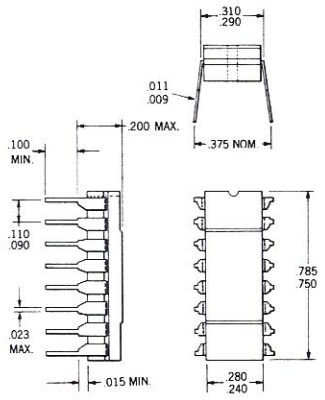
- **20 MHz SHIFT FREQUENCY**
- **TWO INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **CCSL COMPATIBLE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

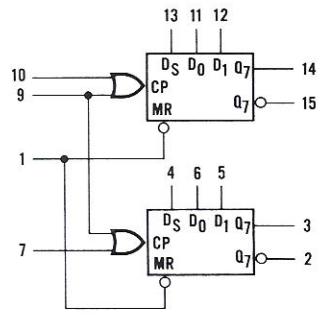
ORDER INFORMATION — Specify U6B9328XXX for 16-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

LOGIC DIAGRAM



Vcc = Pin 16
Gnd = Pin 8

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FAIRCHILD SEMICONDUCTOR
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MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

FUNCTIONAL DESCRIPTION — The two 8 bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 & 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master-slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flop in parallel. When the two clock inputs (the separate and the common) to the OR gate are low, the slave latches are steady, but data can enter the master latches via the R and S input. During the first low to high transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain high. During the high to low transition of the last remaining high clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state; second the data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic high signal. Each 8 bit shift register has a two input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input D_S following the Boolean expression:

Serial data in: $S_D = \overline{D}_S D_0 + D_S D_1$

An asynchronous master reset is provided which, when activated by a low logic level, will clear all sixteen stages independently of any other input signal.

LOADING RULES
(1 U.L. = 1 TTμL input gate load)

INPUT	FAN IN
MR, D_0, D_1	1 Unit Load
Separate CP (pins 7 & 10)	1.5 Unit Loads
D_S	2 Unit Loads
Common CP (pin 9)	3 Unit Loads
OUTPUT	**FAN OUT**
Q_7, $\overline{Q}_7$	6 Unit Loads

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0$ V $\pm 10\%$)

		LIMITS							
		−55°C		+25°C			+125°C		
SYMBOL	CHARACTERISTICS	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5$ V, $I_{OH} = -0.36$ mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5$ V, $I_{OL} = 9.6$ mA $V_{CC} = 4.5$ V, $I_{OL} = 7.44$ mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR, D_0, D_1)		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.5$ V $V_F = 0.4$ V
1.5 I_F	Input Load Current (separate CP pins 7 & 10)		−2.4		−1.5	−2.4		−2.4	mA	
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_R	Input Leakage Current (MR, D_0, D_1)		60		10	60		60	μA	$V_{CC} = 5.5$ V $V_R = 4.5$ V
1.5 I_R	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	
2 I_R	Input Leakage Current (D_S)		120		20	120		120	μA	
3 I_R	Input Leakage Current (common CP pin 9)		180		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	$V_{CC} = 5.0$ V

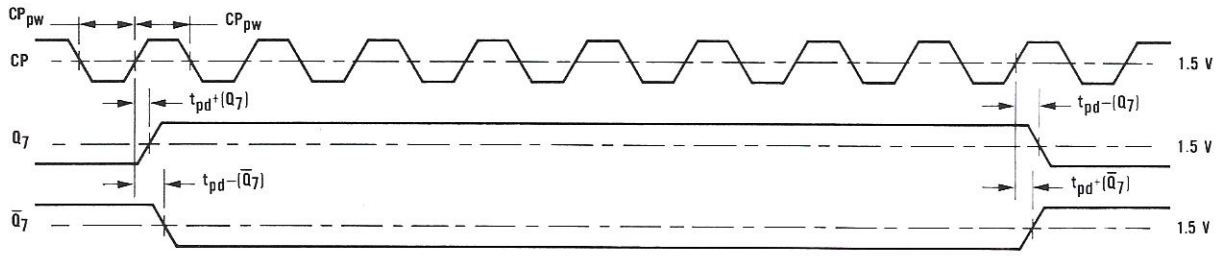
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR, D_0, D_1)		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$1.5\ I_F$	Input Load Current (separate CP pins 7 & 10)		−2.4		−1.5	−2.4		−2.4	mA	
$2\ I_F$	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	
$3\ I_F$	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_R	Input Leakage Current (MR, D_0, D_1)		60		10	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$1.5\ I_R$	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	
$2\ I_R$	Input Leakage Current (D_S)		120		20	120		120	μA	
$3\ I_R$	Input Leakage Current (common CP pin 9)		180		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	$V_{CC} = 5.0\ V$

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

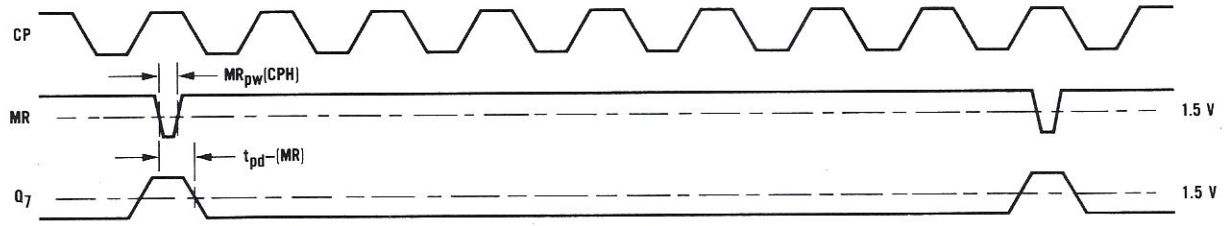
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q_7 & $\overline{Q}_7$)	Turn-Off Delay (clock to output)		13		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 1
t_{pd-} (Q_7 & $\overline{Q}_7$)	Turn-On Delay (clock to output)		22		ns	
t_{pd-} (MR)	Turn-On Delay (Master reset to output)		35		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 2 & 3
CP_{pw}	Min. Clock Pulse Width		14		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 1
MR_{pw} (CPH)	Min. Master Reset pulse width with clock high		15		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 2
MR_{pw} (CPL)	Min. Master Reset pulse width with clock low		28		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 3

SWITCHING WAVEFORMS



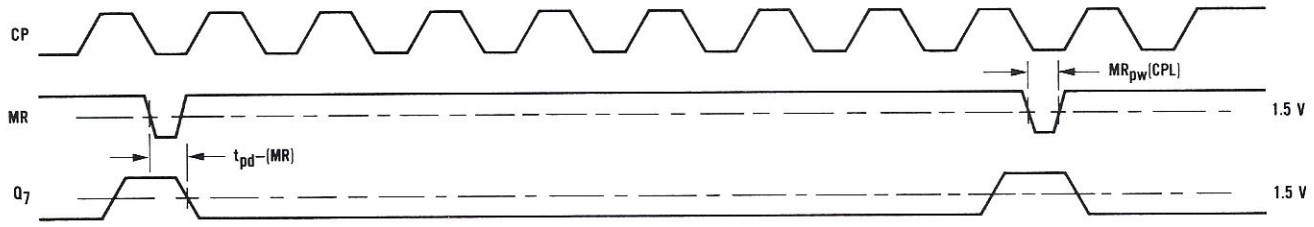
Note: $\overline{Q}_7$ is connected to D_1. Other clock is grounded.

Fig. 1



Note: D_S, D_1, D_0 are high. Other clock input is grounded.

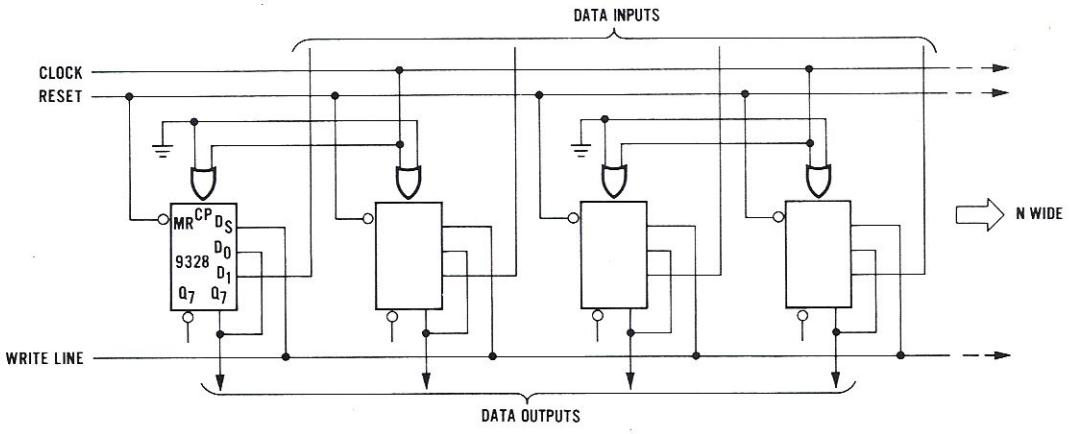
Fig. 2



Note: D_S, D_1, D_0 are high. Other clock input is grounded.

Fig. 3

APPLICATION:



N-BIT BY 8-WORD HIGH-SPEED MEMORY

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